REMARKS

Claims 1-20 were examined and reported in the Office Action. Claims 1-20 are rejected. Claims 1, 6, 11 and 16 are amended. Claims 1-20 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. Claim Objection

It is asserted in the Office Action that claim 16 is objected to because the last line 2 should read "the at least one processor" instead of "the at least processor". Applicant has amended claim 16 to overcome the objection.

Accordingly, withdrawal of the Examiner's objection for claim 16 is respectfully requested.

II. 35 U.S.C. § 112, second paragraph

It is asserted in the Office Action that claims 1-5 and 18 are rejected in the Office Action under the second paragraph of 35 U.S.C. § 112, second paragraph for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as his invention. Applicant has amended claims 1 and 16 to overcome the 35 U.S.C. § 112, second paragraph rejections.

Accordingly, withdrawal of the 35 U.S.C. § 112 rejections for claims 1-5 and 18 are respectfully requested.

III. 35 U.S.C. § 103(a)

It is asserted in the Office Action that claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,181,151 issued to Wasson ("Wasson") in view of U. S. Patent No. 5,701,308 issued to Attaway et al. ("Attaway").

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of "[a]n apparatus comprising: an internal test bus (ITB); a plurality of deskew clusters coupled to the ITB, wherein the plurality of deskew clusters each include a deskew controller; an integrated test controller (ITC) coupled to the ITB, said ITC having an instruction register and a test access port finite state machine (TAP FSM); and a debug unit coupled to the ITC, said debug unit triggers a signal as an input to said ITC in response to an externally generated test signal; wherein the ITC only generates a single global control signal and each of the deskew controllers generates a first local control signal and a second local control signal in response to the single global control signal, where said ITC encodes and transmits states of said TAP FSM and test instructions to at least one logic unit controller over said ITB to test said apparatus, wherein a snapshot instruction and a

shift instruction are partitioned into separate operations and it is not necessary to synchronize the snapshot instruction and the shift instruction."

Applicant's amended claim 6 contains the limitations of "[a] method comprising: generating a single global control signal in an integrated test controller within an integrated circuit in response to an external signal; decoding the single global control signal in a deskew controller in the integrated circuit; generating a first local control signal corresponding to the single global control signal; distributing the first local control signal to a regional clock driver (RCD); and performing one of a debug operation and a testability operation on the integrated circuit by using the single global control signal and the first local control signal, where a snapshot instruction and a shift instruction are partitioned into separate operations and it is not necessary to synchronize the snapshot instruction and the shift instruction."

Applicant's amended claim 11 contains the limitations of "[a] program storage device readable by a machine comprising instructions that cause the machine to: generate a single global control signal in an integrated test controller within an integrated circuit; decode the single global control signal in a deskew controller within the integrated circuit; generate a first local control signal corresponding to the single global control signal; distribute the first local control signal to a regional clock driver (RCD); and perform one of a debug operation and a testability operation on the integrated circuit by using the single global control signal and the first local control signal, wherein a snapshot instruction and a shift instruction are partitioned into separate operations and it is not necessary to synchronize the snapshot instruction and the shift instruction."

Applicant's amended claim 16 contains the limitations of "[a] system comprising: at least one processor; a global bus coupled to the at least one processor; a memory coupled to the global bus; an internal test bus (ITB) located within the at least one processor; a plurality of deskew clusters coupled to the ITB, wherein the plurality of deskew clusters each include a deskew controller; an integrated test controller (ITC) coupled to the ITB; and a debug unit coupled to the ITC; wherein the ITC only generates a single global control signal and each of the deskew controllers generates a

first local control signal in response to the single global control signal to test the at least one processor, wherein a snapshot instruction and a shift instruction are partitioned into separate operations, and it is not necessary to synchronize the snapshot instruction and the shift instruction."

Wasson discloses an integrated circuit (IC) tester. Wasson does not disclose, teach or suggest an ITC only generates a single global control signal and each of the deskew controllers generates a first local control signal and a second local control signal in response to the single global control signal. Moreover, Wasson does not teach, disclose or suggest that a snapshot instruction and a shift instruction are partitioned into separate operations and it is not necessary to synchronize the snapshot instruction and the shift instruction.

Attaway discloses a built in test architecture with an interface that is compatible with IEEE 1149.1. Attaway, however, does not teach, disclose or suggest an ITC only generates a single global control signal and each of the deskew controllers generates a first local control signal and a second local control signal in response to the single global control signal. Moreover, Attaway does not teach, disclose or suggest that a snapshot instruction and a shift instruction are partitioned into separate operations and it is not necessary to synchronize the snapshot instruction and the shift instruction.

Therefore, if Wasson were combined with Attaway the resulting invention would still not contain all of the limitations of Applicant's amended claims 1, 6, 11 and 16 as the resulting invention would not teach, disclose or suggest that an ITC only generates a single global control signal and each of the deskew controllers generates a first local control signal and a second local control signal in response to the single global control signal, nor that a snapshot instruction and a shift instruction are partitioned into separate operations and it is not necessary to synchronize the snapshot instruction and the shift instruction.

Since neither Wasson, Attaway, nor the combination of the two disclose, teach or suggest all the limitations contained in Applicant's amended claims 1, 6, 11 and 16, as listed above, there would not be any motivation to arrive at Applicant's claimed

invention. Thus, Applicant's amended claims 1, 6, 11 and 16 are not obvious over Wasson in view of Attaway since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from claims 1, 6, 11 and 16, namely claims 2-5, 7-10, 12-15, and 17-20, respectively, would also not be obvious over Wasson in view of Attaway for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 1-20 are respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-20, patentably defines the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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Dated: April 6, 2004

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on April 6, 2004.

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Nadya Gordon